Reduced Implementation of D-Type DET Flip-Flops
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Abstract—One of the main disadvantages of using D-type double-edge triggered flip-flops (DET-FF's) in VLSI systems design is the number of transistors required. In this paper two new DET-FF circuits (one static, the other dynamic) are proposed in which the number of transistors is reduced to a number similar to that for classic single-edge triggered flip-flops (SET-FF's). Both new circuits not only behave correctly when operated at high frequency but also offer a good level of immunity to metastability problems (static) and race problems (dynamic), as well as presenting a simple straightforward layout. These considerations offer wider practical and economic applications for the use of DET-FF's in VLSI systems design.

I. INTRODUCTION

The advantage of using edge-triggered flip-flops in VLSI systems design is well known. With this technique the setup time for data input is independent of the clock-pulse width, and the circuit implementation is a great deal simpler. One drawback, however, is that the flip-flops normally used in digital system design change their output only on one of the two clock edges, hence leaving idle a part of the circuit during one of the two clock transitions, although changes do occur in parts of the elements inside the flip-flop. The extra power consumption and time cost of single-edge triggered flip-flops (SET-FF's) may therefore have a decisive influence on future CMOS VLSI design developments.

Double-edge triggered flip-flops (DET-FF's) in digital circuit design, on the other hand, reduce power consumption and increase data movement to twice its speed compared with SET-FF based design. Their main disadvantage, however, as reported in [1]-[3], is the substantial increase in the number of transistors required to implement each flip-flop. The circuit proposed in [2] for a static D-type DET-FF needs a minimum of 26 MOS transistors, while 20 transistors are necessary for the dynamic circuit proposed in [3]. Furthermore, these circuits may present some metastability problems, in the static case [4], slow response time as reported in [2], and malfunction when output is applied to precharge dynamic circuits [3].

The dynamic and static CMOS implementations for D-type DET-FF's that we propose require a minimum number of MOS transistors (similar to those used in typical SET-FF's). These circuits (see Sections II and III) have been designed for maximum logic excursion, high-speed operation, and prevention of metastability and race problems for the static and dynamic circuits, respectively. The results are circuits with layout simplicity and modularity.

Fig. 1. (a) Module A and (b) module B of proposed static D-type DET-FF.

II. NEW STATIC CIRCUIT DET-FF DESIGN

The static circuit design is shown in Fig. 1. Only 16 MOS transistors are needed, grouped into two modules, A and B, each with a clocked inverter as input buffer and a memory block composed of two clocked inverters. The behavior of both modules is multiplexed through transistors M5-M8. At each clock transition the input buffer of one module and the memory block of the other are driving, while the two remaining circuit elements stay idle. For example, when clock CLK is at low level, module B's input buffer and module A's memory block are driving, thus node N7 is loading inverted input. Since node B's memory block is not driving, output Q does not affect node N7. Output Q, on the other hand, is maintained by module A's memory block. If clock CLK switches to high level, the value loaded in node N7 will determine a new value in output Q.

If the values stored in node N7 and output Q are equal, a conflict could arise for the new Q value in the next clock switch. It is therefore essential, for correct circuit performance, that the conductivity of the inverter formed by M15 and M16 be less than that of M11 and M12, thereby guaranteeing that node N7 will fix the new Q value. If this conductivity difference is not taken into account the circuit may operate incorrectly.

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Several analyses have shown that the best way of implementing the different conductivity is to increase the channel length of transistors $M_{15}$, $M_{16}$, $M_{13}$, and $M_{14}$. Fig. 2 shows how the flip-flop time-delay average varies in relation to the channel length of these transistors. Except for the aforementioned transistors, the remainder may be of minimum size ($w = 4 \, \mu m, l = 1.6 \, \mu m$) unless one wishes to improve the time response, in which case the conductivity of the clocked transistors must be increased. The sizes found to be optimum are shown in Fig. 1.

In flip-flops reported to date, once the clock has switched and after a short time hold, the input has no influence over the output. Hence, if a metastable voltage has been stored, the time resolution is not dependent on what happens in the input. This does not occur in the proposed new DET-FF's. Let us suppose that CLK is low, $V_{N_{5}} = V_{Q} = V_{m}$ (metastable voltage), and $D$ is low; under these conditions $M_{5}$, $M_{3}$, $M_{15}$, and $M_{1}$ are driving, which tends to reduce the voltage of the output node and to cause a lower time resolution. Moreover, the output tends towards the correct value. It should also be noted that if the flip-flop is functioning correctly, some of these transistors are off; this is a clear advantage for any synchronizer.

III. NEW DYNAMIC DET-FF CIRCUIT DESIGN

There are several well-known techniques for SET-FF's design. These are: by transmission gates, by inverters with clocked transistors connected to supply rails, by dynamic inverters with three transistors [3], and by inverters with clocked transistors connected to output.

Starting from these techniques, we have studied and evaluated different prototypes of dynamic DET-FF implementations. The first two implementations (by the two first techniques) malfunction because of charge sharing in the output node. The implementation proposed in [3], carried out with three levels of dynamic inverters, presents the problem of signal disturbances in the output if, when the clock switches, the input remains unchanged.

The dynamic DET-FF circuit we propose, Fig. 3, is based on the connection of two dynamic D-type SET-FF's grouped into two modules, $A$ and $B$, each built with two clocked inverters, requiring a total of 14 minimum-size MOS transistors.

For this circuit, in each clock level, only the clocked input inverter of one module is active while the output inverter of the same module remains in a state of high impedance. In the other module, the input inverter remains in a state of high impedance and the output inverter is active. At the clock transitions, the precharged values in the drains of the transistors connected to the power rails are transmitted to the corresponding output of the clocked inverters that are switching to the active state. This operation indicates that the new output value on each clock edge has to pass through a single transistor to reach the output; so the transition time will be short. The symmetrical behavior of both modules guarantees the double edge trigger of the proposed circuit.

The new design avoids charge sharing, consequently the charge stored in the output of the clocked inverters remains there for considerably more time than for other implementations (Table I). On the other hand, in Fig. 4, we can see the shorter transition width of this circuit (approximately 1.65-2.1 V) compared with that of the dynamic circuit proposed in [3] (approximately 1.4-3.1 V).

With regard to race problems due to skew between the two clock phases, the circuit behavior performed correctly and, as was also reported in [6], supported a skew interval of over 2.5 ns, which is considerably superior to the real skew produced by obtaining the inverted clock signal with a local inverter.

IV. RESULTS AND CONCLUSIONS

The two circuits proposed in this paper were simulated using 1.5-$\mu m$ CMOS technology and an HSPICE simulator at level 6. The static circuit behavior was simulated at several clock frequencies and maintained a correct performance at frequencies superior to 250 MHz (see Fig. 5(a)) equivalent to 500 MHz in the SET-FF's. The dynamic circuit was also sim-
Table I shows the behavior of the circuits proposed in this paper and several circuits proposed in recent literature [2], [3].

In conclusion, two new minimum CMOS circuits are proposed in this paper, one static and the other dynamic, for double-edge triggered flip-flops. The circuits have been designed specifically to reduce the number of transistors, to maintain maximum excursion logic, to obtain high-frequency operations, and to offer a good level of immunity to problems of metastability (static) and race (dynamic).

REFERENCES


