extended if the normalisation factor, \( i_n \), is varied with respect to \( i_i \). This feature is of particular interest in low-voltage circuits.

The principles of the current divider circuit may be exploited to perform complex arithmetic operations. For example, Fig. 4 shows a circuit that incorporates switched current circuitry and the proposed divider circuit to implement the function \( V_{C2} = k(i_x/i_y + i_x/i_z) \), where \( k = C_1 V_o/C_2 \). Fig. 4 also includes the timing diagram to illustrate the operation of this circuit. In the positive half of the clock cycle, \( i_x \) charges \( C_2 \) until \( i_z \) charges \( C_3 \) to raise \( V_{C1} \) to \( V_a \). When \( V_{C1} = V_a \), capacitor \( C_3 \) ceases to charge as transistor \( M_1 \) is turned off by the comparator output voltage \( V_T \). The output voltage is therefore maintained at \( k(i_x/i_y + i_x/i_z) \). The time duration, \( T_{DH} \), for charging \( C_1 \) in the positive half of the clock cycle is governed by the quantity \( C_1 V_o/i_x \). Any time after \( T_{DH} \), \( M_1 \) is switched off, \( V_{C1} \) may be reset via reset-1, while \( V_{C2} \) sustains the previous voltage. At the start of the second reset-1 pulse, the clock enters the negative cycle from which the input currents are switched such that \( i_x \) charges \( C_3 \) and \( i_z \) charges \( C_1 \). Once \( V_{C1} \) reaches \( V_a \) during the negative half of the clock cycle, capacitor \( C_3 \) will have acquired a change in output voltage given by \( \Delta V_{C2} = k(i_z/i_y) \). Hence, at the end of a clock period, the function \( V_{C2} = k(i_x/i_z + i_x/i_z) \) is realised.

**Fig. 4** Example circuit including signal waveforms to implement function \( V_{C2} = k(i_x/i_z + i_x/i_z) \)

At end of \( T_{DH} \) output voltage is proportional to \( i_x/i_z \), and at end of \( clk \) period output voltage is proportional to \( i_x/i_z + i_x/i_z \)

**Conclusion:** A very simple circuit for performing current division has been proposed. This circuit operates at low currents and does not require any device matching; hence, the operation of this circuit is robust. Dedicated to low-power and low-voltage applications, the proposed divider circuit offers simplicity as it is composed of few devices and occupies a small silicon area. Several specific applications of the current divider in current-mode signal processing have been suggested to demonstrate the versatility of the proposed circuit.

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**DC side harmonic reduction in rectifiers by direct ripple reinjection**

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A new technique for eliminating DC side harmonics in rectifiers is proposed, based on the direct reinjection of the voltage ripple in series with the DC line. The operation of the proposed scheme is analysed and provides experimental verification in a 12-pulse scaled down model of a converter.

**Introduction:** Passive filters are commonly used to reduce the level of DC side harmonics in AC/DC converters [1]. However, this is an expensive solution, and therefore normally restricted to the elimination of the first harmonic as this harmonic has the highest value. Active and passive filters have recently been successfully combined to reduce the higher harmonic content [2].

In this Letter we describe an alternative solution to the use of passive and active filter arrangements on the DC side of the converter. It shares with active filters the principle of active cancellation of the harmonic content, but differs from it in that processing and amplification are not necessary, and in the use of voltage rather than current harmonic cancellation.

**Harmonic voltage source:** A rectifier normally connects a relatively low impedance (of the AC system) with a large smoothing reactor (on the DC side). Under these conditions the converter acts, when viewed from the DC side, as a source of harmonic voltages.

**Fig. 1** Schematic circuit of voltage reinjection scheme

**Description of voltage reinjection scheme:** The ripple reinjection circuit, shown in Fig. 1, consists of a 1:1 ratio reinjection transformer \( T \), with the primary winding of \( T \) being in series with a capacitor \( C \), and the secondary winding of \( T \) in series with the DC output voltage. The output voltage of the reinjection circuit is proportional to the sum of the input current and the DC voltage applied to the primary winding. The output voltage is then injected into the DC side of the converter, effectively reducing the harmonic content of the DC voltage. The proposed scheme is robust and operates at low currents, requiring no device matching. It is particularly useful for low-power and low-voltage applications, where the simplicity and small silicon area are advantageous. Several specific applications of the current divider in current-mode signal processing have been suggested to demonstrate the versatility of the proposed circuit.
output. The capacitor is used to block the DC voltage and, if C is sufficiently large, most of the ripple content \( V_d \) will be transferred to the reinjection transformer, which will in turn provide an opposing voltage source \(-V_e\) in series with the DC output.

It should be noted that the transformer secondary winding, which is in series with the line, will carry the full DC current and the core of the transformer must be of a dimension such that saturation will be avoided. Compared with the active filtering alternative [2], in this scheme the harmonic source (in this case a harmonic voltage) is eliminated rather than the effect of the harmonic source (i.e. a harmonic current). There is no need for waveform capturing, processing and signal amplification [3, 4].

In the circuit of Fig. 1, the load voltage is the sum of two components: one is the mean DC voltage and the second \( V_d \) the remaining ripple content, which is the difference between \( V_d \) and \( V_e \).

Considering only the AC components, since the DC voltage is blocked by the

\[
V_d = V_a - V_e \quad (1)
\]

\[
V_e = V_a + V_b \quad (2)
\]

or

\[
V_d = V_a + V_b - V_e = 0 \quad (3)
\]

Eqn. 3 indicates that the unfiltered ripple content is equal to the capacitor voltage drop and should therefore reduce in proportion to the capacitor size.

Analysis of reinjection circuit and selection of blocking capacitor:

Applying mesh analysis to the circuit of Fig. 1 produces the equations

\[
V_d(s) = \left( \frac{1}{C s} + L s \right) I_1(s) + M s I_2(s) \quad (4)
\]

\[
V_e(s) = M s I_1(s) + (L s + L_d s + R) I_2(s) \quad (5)
\]

When \( s = j \omega \)

\[
X_1 = j \omega L \quad X_m = j \omega M \quad X_{LC} = j \omega C \quad X_e = -\frac{j}{\omega C} \quad (6)
\]

If \( X_1 = X_e \), eqns. 5 and 6 can be solved in terms of \( I_2 \) to give

\[
I_2 = \frac{V_e}{X_m} \quad (7)
\]

\( I_1 \) can be a large current, considering that \( X_m \) (the transformer mutual coupling reactance) will be relatively low compared to the impedance of the DC transmission link.

According to eqn. 3, a complete harmonic cancellation would require infinite capacitance. For a cost effective solution the harmonic levels must stay below certain specified limits. To meet this condition the natural resonance offered by the combination of the capacitor and the reinjection transformer must occur at a frequency well below that of the lowest expected characteristic harmonic.

The criterion used here for the selection of the capacitor is to prevent the amplification of any harmonic frequency down to the fundamental, which is achieved when

\[
C > \frac{1}{\omega_0^2 L} \quad (8)
\]

where \( \omega_0 = 2\pi f \) and \( f \) is the fundamental frequency of the AC system; using the parameters of the system described in the following Section, the above condition is satisfied with a 112.5µF capacitor.

The load voltage \( V_d \) against frequency when the value of the capacitor is varied has been determined for the test system using PSPICE with a source of 100V peak. The results are shown in Fig. 2 for capacitor values from 100 to 500µF and values of load similar to those that will be used in the real circuit. At very low frequencies, the use of a capacitor below 112.5µF amplifies the original voltage slightly. However, the transfer of the harmonic voltages reduces rapidly for increasing frequencies. The use of larger capacitors further reduces the transfer function, although the incremental reduction becomes insignificant for frequencies beyond 300Hz.

Experimental verification: The operating principle of the reinjection scheme has been verified in a 12-pulse scaled down converter, windings to the 380V power supply with a 500Ω, 0.1 H resistive-inductive load.

The inductance and resistance of the two reinjection transformer windings are 0.09H and 40Ω and the core of the transformer was designed to provide a linear magnetising characteristic for a 240 peak voltage level.

As discussed in the preceding Section, the blocking capacitor required to avoid any ripple amplification down to the 50Hz frequency, has a value of 112.5µF and the actual capacitor selected for the test system is 141µF.

Fig. 2 Simulated response of reinjection scheme to harmonic source of 100 V (peak)

Fig. 3 Ripple voltages measured with and without reinjection circuit

Waveform and spectrum are shown

- \( a \) DC voltage output from AC/DC converter
- \( b \) Converter output with voltage ripple reinjection

Fig. 3a and b illustrate the ripple voltages measured without and with the reinjection circuit for a firing delay angle of 15°. Considerable reductions are noted, both in the characteristic and non-characteristic harmonics with the reinjection circuit in service, particularly at higher harmonic frequencies. Referring to the frequency spectra and in particular to 300Hz (the first characteristic
harmonic) the ripple voltage reduces to ~20%. At the low end of the spectrum the effectiveness of the scheme gradually reduces; for instance, the 75Hz component, present in the experimental system, is only halved.

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Fast lock-on time mixed mode DLL with
10ps jitter
Seon-Ho Han, Joo-Ho Lee and Hoi-Jun Yoo

A fast lock-on time mixed mode delay locked loop (DLL) is
proposed to eliminate phase error in two steps. A digital fixed
delay line compensates for the initial large phase error and an
analogue voltage controlled delay line compensates for the small
static phase error, resulting in low jitter. The lock-on time of the
DLL is less than 10 clock cycles and the simulated jitter is below
10ps at 200MHz.

Introduction: Phase locked loops (PLLs) and delay locked loops
(DLLs) are widely used to omit clock skew in synchronous
DRAM and high speed interface applications [1–6]. These loops
have a low jitter as well as a fast lock-on time. Other clock
synchronisation circuits such as SMD and RDL have been developed
for SDRAM and high speed interface applications because of their fast lock-on characteris-
tics [1–3]. However, the phase error of these circuits is relatively
large compared to that of PLLs or DLLs.

Fig. 1 Architecture of mixed mode DLL

In this Letter, we present a mixed mode DLL with which both a
fast lock-on time and low jitter are possible. In a conventional
architecture, it is difficult to predict the final voltage value of the
locked $V_{cl}$ (control voltage of the voltage controlled delay line
(VCDL)). Therefore, the current mismatch resulting from the
$V_{cl}$ difference between the PMOS and NMOS of the charge pump end
driver generates a static phase error when the DLL loop locks.
Also, conventional DLLs have a long lock-on time. The proposed
mixed mode DLL solves such problems by two locking steps,
compensating for the large skew between $e_{cb}$ and $i_{cb}$ and then
compensating for the fine skew.

Circuit description: Fig. 1 is a block diagram of the mixed mode
DLL. It is composed of an analogue VCDL and a digital fixed
delay line (FDL). The analogue part is composed of a phase
frequency detector (PFD), an internal clock detector (ID), charge
pump (CP), 1/2 $V_{cc}$, generator and a VCDL. The VCDL block is
composed of a differential voltage controlled delay cell and replica
biasing circuits. The $V_{cl}$ of the mixed mode DLL has a value near
$V_{cc}/2$ because the phase error between $e_{cb}$ and $i_{cb}$ is very small
(one FDC unit delay). It is possible for the charge pump driver to
be optimised for current matching to obtain a low static phase
error, resulting from the negligible $V_{cl}$ mismatch of the charge
pump end driver. Fig. 2a shows the simulated $V_{cl}$ waveforms of
the conventional VCDL and mixed mode DLL. The lock-on times
of the conventional VCDL and the mixed mode DLL are 0.44μs
and 40ns, respectively.

Fig. 2 Simulation waveforms at 200MHz

(a) Conventional VCDL
(b) clock synchronisation waveforms

The digital part of the DLL is composed of a monitor (clock
driver), TDC (time to digital converter) and a digital to time con-
verter (DTC) [3]. In the initial state, the control voltage of the
VCDL is maintained at $1/2$ $V_{cc}$ and the ID disables the PFD. Each
digital delay cell (DDC) unit in the TDC and DTC is composed
of an inverter and a NAND gate. In this study the unit delay is
174ps, which determines the initial static phase error of the fol-
lowing analogue VCDL.

Fig. 3 Timing diagram of mixed mode DLL

Fig. 3 shows the timing diagram obtained at a low frequency.
For exact locking, the following equation should be satisfied:

$$T_{clk} = t_{VCDL} + t_{monitor} + t_{comp}$$

where $t_{monitor}$ is the delay of the replica driver, $t_{comp}$ is the delay
time compensated for by the FDL in the initial step, and $t_{VCDL}$(constant)
is the constant delay of the VCDL at $V_{cl} = 1/2$ $V_{cc}$. After two clock cycles $t_{monitor} + t_{comp} + t_{VCDL}$(constant) is obtained to
synchronise $i_{cb}$ with $e_{cb}$, and then $t_{VCDL}$ is optimised by the
anologue DLL locking process to obtain low jitter.

Simulated performance: A mixed mode DLL circuit was designed
using a 0.4μm CMOS technology. Fig. 4 shows the simulated jitters.

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