A soft-solution electrochemical processing technique for preparing CdTe/n-Si(1 0 0) heterostructures

H. Gómez a,*, R. Henríquez a, R. Schrebler a, G. Riveros a, D. Leinen b, J.R. Ramos-Barrado b, E.A. Dalchiele c

a Instituto de Química, Facultad de Ciencias, Universidad Católica de Valparaíso, Casilla 4059, Valparaíso, Chile
b Departamento de Física Aplicada & Ingeniería Química, Facultad de Ciencias, Universidad de Málaga, E29071 Málaga, Spain
c Instituto de Física, Facultad de Ingeniería, Herrera y Reissig 565, C.C. 30, 11000 Montevideo, Uruguay

Received 13 January 2004; received in revised form 13 July 2004; accepted 17 July 2004

Abstract

The rear side of an n type (1 0 0) Si wafer polished on one side was chosen as a substrate for CdTe thin film electrodeposition because its high density of surface non-uniformities is expected to result in a macroscopic equalization of injection conditions for electrons along the surface and subsequent uniform deposit growth. The films were grown from a plating bath containing 5 mM TeO2, 0.5 M CdSO4, 0.5 M H2SO4 and 0.5 M NH4F at a temperature of 85 °C. The deposition potential was selected after studying the electrochemical behavior of the precursors by cyclic voltammetry. EDS analysis showed that films with near stoichiometric composition were obtained at ca. 0.575 V vs SCE. XRD showed that the as deposited films are well crystallized with a preferential orientation along the [1 1 1] cubic direction, whereas AFM images show uniform and compact morphology. XPS results revealed that Te–O bonds, mainly in the surface, are also present.

© 2004 Elsevier B.V. All rights reserved.

Keywords: CdTe; Si; Electrodeposition

1. Introduction

Formation of semiconducting chalcogenide compounds thin film/single crystal semiconductor heterostructures is very important both technologically and scientifically, presenting many applications in optoelectronics and in highly efficiently solar cells [1]. As was expressed by the 2000 Physics Nobel Prize winner Zhores I. Alferov: “It is impossible to imagine now modern solid-state physics without semiconductor heterostructures” [2].

Chalcogenide cadmium telluride (CdTe) is recognized as a highly versatile narrow bandgap binary compound semiconductor \( E_g = 1.45 \text{ eV} \) [3], which is the only binary II–VI material that can be found both in n- and p-conductivity types [4,5]. Furthermore, its direct optical transition results in a large absorption coefficient, making possible its use in thin-film solar cells. Other applications include gamma-ray and infrared detectors [6]. Its close lattice match and chemical compatibility with HgCdTe makes CdTe an ideal substrate for growth of this variable band-gap infrared detector material [7,8]. Lately, these materials are generating great interest because their properties are well suited for the fabrication of nuclear radiation detectors operating at room temperature [9].

On the other hand, silicon is appealing as a substrate material due to its transparency to infrared radiation out to wavelengths beyond 14 µm and because...
large-area wafers of the highest structural perfection are readily available commercially at a minimal cost. Besides, Si integrated circuit processing technologies are well developed and can be combined readily with selected area HgCdTe hybrid infrared focal plane arrays (IRFPAs) [7], purportedly to be used in very large applications in military, space and medical imaging areas for infrared imaging and low-background detection. However, the different natures of the two materials create some specific difficulties when CdTe is grown on silicon substrates. Among these, the cubic lattice constant of Si is 5.43 Å while that of CdTe is 6.48 Å [11], which amounts to a lattice mismatch of about 20% at 25 °C. This very large lattice mismatch is expected to generate many dislocations at the interface, which must be prevented from propagating into the active part of the layer. Besides, when the layer is cooled down from the growth temperature, additional strains and dislocations are caused by the thermal mismatch between CdTe and Si (thermal expansion coefficient difference Δα/α ≈ 46.9% at 25 °C) [10]. This problem would be less severe if a lower CdTe growth temperature could be used.

Various growth techniques, such as molecular-beam epitaxy (MBE) [10,12,13], metal/organic chemical vapor deposition (MOCVD) [14–16], UHV sublimation [16], metal/organic vapor phase epitaxy (MOVPE) [17] and hot wall epitaxy [18,19] have been used to grow CdTe films onto silicon substrates. Notwithstanding, some problems due to the high temperature growth process are mentioned in the literature. For example, films grown by UHV sublimation method at a substrate temperature below 250 °C exhibited streaked X-ray diffraction patterns which contained extra hexagonal-phase features due to the presence of stacking sequence errors [16]. Similar results have been reported also by Holt and Abdalla [20], who deposited CdTe onto [1 1 1] Si substrates using electron evaporation techniques. Growth routes using gaseous phases require even higher energy than standard high-temperature processes and have resulted in environmental problems because the energy consumed results in exhausted gas(es) or exhaust heat (entropy) [21,22].

Low-temperature, in situ fabrication of crystalline thin films, is essential in order to improve their quality, lower production costs, and make the whole process environmentally friendly. In this sense, soft-solution processing (SSP) techniques of thin film preparation appear as an interesting alternative route to achieve these goals. They can be defined as environmental friendly processing using aqueous solutions that seem to provide results similar to other processes using fluids (such as vapor, gas, and plasma) or beam/vacuum processing, while consuming less total energy than other processing routes [21,22]. Electrodeposition is a typical “soft-solution processing” application, which can be more accurately designated as a soft-solution electrochemical processing (SSEP), which enables the formation of semiconductor thin films from an aqueous solution at T = room temperature – 100 °C under atmospheric pressure. SSEP is a relatively low energy process compared with other methods such as conventional thin film growth techniques. In addition to their low cost and their capability of controlling composition and morphology by electrochemical parameters, the advantage of working in the low temperature domain is very attractive as soon as inter-diffusion phenomena found at high temperatures become critical, as for example, for thin film II–VI compounds. SSEP is orthogonal to the heat based methods; it is based on controlling the activity of electrons, not the temperature of the substrate and reactants [23]. Besides, in the literature there are some examples of as grown electrodeposited semiconductor thin films with good structural and optoelectronic properties, without further annealing [24–26]. Another important advantage of electrodeposition is that the driving force of the reaction is precisely known and controlled. Furthermore, since the current is proportional to the deposition rate, the current-time transient following a potential step provides an in situ measure of the deposition process. Besides, the integral of the current-time transient measures the amount of material deposited, while the shape of the transient indicates the nucleation and growth mechanism [27].

Formation of compound semiconductors by SSEP techniques has been well demonstrated by numerous research groups. The electrodeposition of II–VI and III–V compounds is reviewed in a number of articles [28–30]. These semiconductors are usually plated onto a metal substrate, typically titanium, gold or stainless steel and in some cases onto ITO(Sn-doped In2O3)/glass. Other than oxides, CdTe is the most extensively electrodeposited compound semiconductor; more than 300 studies are concerned with electrodeposition of this II–VI compound. Moreover, although deposition of CdTe on metal surfaces from aqueous or non-aqueous solutions has been extensively studied, little work has been done on electrodeposition onto foreign semiconductor single crystal substrates. Electrochemical growth of CdTe compound semiconductor onto a semiconductor substrate is highly desirable. Table 1 gives a listing of CdTe thin films which have been deposited onto semiconductor single crystal substrates by a SSEP technique. It can be seen that the monocryalline semiconductor sub-

---

2 At this point it must be pointed out that although porous silicon is not a monocryalline semiconductor, it was included in Table 1, due to its importance and as directly derived from silicon and therefore integrated with it.
Electrodeposition on to Si is very difficult, the quality of the Si substrate surface greatly influences the quality of the subsequent layers. For instance, the native oxide formation leads to passivation problems. In order to avoid adventitious surface oxide formations as well as to eliminate the spontaneous deposition of tellurium on the Si surface, meticulous care has to be taken in preparing the Si surface prior to electrodeposition. Accordingly, the difficulty of obtaining good quality CdTe thin films by SSEP onto Si appears to be a great challenge.

The Berlouis group [33,34] and Sugimoto and Peter [36,37] investigated CdTe electrodeposition onto silicon single crystals. Not very satisfactory results were obtained as the electrodeposited film characterization revealed that they do not form either a coherent layer or a preferential crystallographic orientation. Evidence for a 2D nucleation and growth mechanism was obtained by Sugimoto and Peter [36], but the formation of an amorphous deposit was not compatible with an epitaxial growth. More recently, Takahashi et al. [38], presented results on epitaxial growth of CdTe films by electrodeposition onto Si(1 1 1), assisted by pulsed light (from a xenon lamp).

Formation of a homogeneous film can be reached with an ideally energetically uniform surface, a condition that, in practice, is unreachable. An alternative approach can be explored, which consists in using a substrate with a very high density of surface non-uniformities [39]. This approach is expected to result in a macroscopic equalization of injection conditions for electrons all along the surface, resulting in a uniform deposit growth. A very interesting electrochemical characterization of this rough face of Si(1 1 1) in NH₄F solutions was done by Allongue et al. [40].

Moreover, several studies are now in progress in order to reduce the reflectivity of silicon surfaces by textures processing. [41,42]. This is of great importance as it will be possible to reduce solar cell thickness down to a few tens of microns [42]. One of the two most commonly studied and produced texture structures is inverted pyramids [41] that are present in the rear face of silicon polished on one side.

In this context, in the current work we propose to use the rough face side of a n-type (1 0 0) silicon wafer for the electrodeposition and characterization of CdTe thin films.

2. Experimental

Electrodeposition was performed on (1 0 0) monocristalline n-type silicon (1.0–5.5 Ω cm, p-doped, Int.
Wafer Service, CA, USA). n-type silicon was chosen because the n-type character gives a nonblocking electrode for cathodic reactions in dark conditions. The silicon wafer was cut in small 1 \times 1 \text{cm}^2 squares that were first degreased in boiling isopropanol, then rinsed with a 0.5:1:4 HCl:H_2O_2:H_2O mixture heated up to 80 °C, in order to remove any trace of heavy metals. Afterwards, the oxide film was removed by etching with a 2 M NH_4F acid (pH 4.5) solution and thoroughly rinsed with ultra pure water. The ohmic contact was made through the application of a Ga–In eutectic in the polished face of the samples that were mounted in a copper support. The edges of the silicon squares and the copper were isolated with an adhesive Teflon tape leaving a defined exposed area facing the solution. Before the electrochemical experiments, the electrode surface was again etched for 15 min with the 2 M NH_4F solution (after this procedure an atomically smooth and hydrogen terminated surface would be obtained [43,44]).

The electrolytic solutions were prepared from analytical grade reagents with the following compositions: 5 mM TeO_2 + 0.5 M H_2SO_4; 0.5 M CdSO_4 + 0.5 M H_2SO_4; 5 mM TeO_2 + 0.5 M CdSO_4 + 0.5 M H_2SO_4; 5 mM TeO_2 + 0.5 M CdSO_4 + 0.5 M H_2SO_4 + 0.5 M NH_4F.

Cyclic voltammetry experiments were made at room temperature and in dark conditions. The electrolytic solutions were de-aerated prior to the experiment by purging with 5 N nitrogen and, during the measurement, nitrogen was passed over the electrolyte in order to keep the cell atmosphere free of oxygen. A platinum wire served as the counter-electrode and a saturated calomel electrode was used as the reference. The electrodeposition of the Cd + Te films was carried out from a plating bath containing 5 mM TeO_2 + 0.5 M CdSO_4 + 0.5 M H_2SO_4; 5 mM TeO_2 + 0.5 M CdSO_4 + 0.5 M H_2SO_4; and without stirring. The temperature was kept at 85 °C. In order to minimize the formation of a Te layer at the point of working electrode immersion into solution the potential was set at \(-0.200 \text{ V}\) employing a platinum probe.

The electrochemical measurements were done using model IM6e BAS-ZAHNER impedance measurement unit, and electrodepositions were carried out using a model 263A EG&G Princeton Applied Research electrochemical potentiostat.

Powder X-ray diffraction spectra of films were recorded with a Philips PW3710 diffractometer using Cu Kα radiation. The accelerating voltage was set at 40 kV with a 25 mA flux. Scatter and diffraction slits of 1° and a 0.1 mm collection slit were used.

Quantitative standardless microanalyses were obtained using energy dispersive X-ray analysis (EDS) with a JEOL JSM-5410 apparatus. The AFM images were obtained with a Digital Instrument (NANOSCOPE IIIA Series) using the contact mode at a scan rate of 0.02 μm/s.

XPS measurements were made with a PHI 5700 spectrometer equipment using Mg Kα radiation (1253.6 eV) and Al Kα radiation (1486.6 eV) as excitation sources. Spectra were recorded at a 45° take-off-angle with a concentric hemispherical energy electron analyzer operating in the constant pass energy mode at 29.35 eV, using a 720 m diameter analysis area. Under these conditions, the Au 4f7/2 line was recorded with 1.16 eV FWHM at a binding energy of 84.0 eV. The spectrometer energy scale was calibrated using Cu 2p3/2, Ag 3d5/2 and Au 4f7/2 photoelectron lines at 932.7, 368.3 and 84.0 eV, respectively. The pressure in the analysis chamber was maintained lower than ~10–7 Pa. The PHI ACCESS ESCA-V6.0 F software package was used for data acquisition and analysis. The atomic concentrations were calculated from the photoelectron peak areas using Shirley [45] background subtraction and sensitivity factors provided by the spectrometer manufacturer (Physical Electronics, Eden Prairie, MN). Recorded spectra were calibrated in binding energy according to Cd 3d5/2 at 404.9 eV [46]. Sputtering was carried out using 4 keV Ar⁺ bombardment at a current density of 3 μA cm⁻². A sputter rate of 0.5 nm/min was determined for Ta₂O₅ under the same sputter conditions.

Scanning electron microscopy (SEM) pictures were obtained on a JEOL JSM-5300 apparatus.

3. Results and discussion

3.1. Topography of the silicon rough surface

In order to understand further electrochemical results, the morphology characterization of the rear side of the single polished side n-Si(1 0 0) wafer (the rough surface) was done by SEM analysis. Fig. 1 shows its structure as received, where the presence of inverted truncated square pyramidal structures fully covering

Fig. 1. SEM micrograph of the rear side of the n-(1 0 0) Si surface polished on one side.
the silicon surface can be observed. This pyramidal texturing can be attributed to the combination of anisotropic etching of the silicon, and to hydrogen bubbles evolved during the etching reaction [41].

3.2. Voltammetric study

Fig. 2 presents an energy band diagram for n-Si(1 0 0) in 0.5 M H₂SO₄, assuming a reorganization energy of 1 eV. The flatband potential in this solution, determined from Mott–Schottky plots (results not shown) is −0.259 V vs. SCE. From the donor density, the position of the conduction and valence band edges at the surface were determined to be −0.529 and +0.581 V, respectively. The reduction of HTeO₂⁺ to Te⁰ is a four electron process:

\[
\text{HTeO}_2^+ + 3\text{H}^+ + 4\text{e}^- \leftrightarrow \text{Te}^0 + 2\text{H}_2\text{O}
\]  

with an equilibrium potential, \( U_{\text{eq}}^0 = +0.278 \text{ V vs SCE} \).

From the energy diagram band, it can be seen that the equilibrium potential of the HTeO₂⁺/Te⁰ couple is shifted to sufficiently high energy meaning that Te electrodeposition is expected to occur via electron transfer from the conduction band into the chalcogen ion states. As the density of the conduction band electrons is determined by the band bending, this deposition process is dependent on the applied potential, so that an external control over the latter can be achieved. Furthermore, by avoiding overlap of the tellurium ion acceptor states with the silicon valence band, electroless deposition (by hole injection into the valence band of the silicon substrate) can be prevented. Fisher et al. [33] consider that it is cadmium and not tellurium that undergoes a deposition reaction by hole injection into the silicon valence band. Therefore, the electroless plating of Te onto silicon, which has been reported in previous work, can be explained by a subsequent cadmium corrosion reaction that provides the necessary electrons for the tellurium deposition [33]. Accordingly, it can occur only when silicon is in contact with a solution containing both Cd and Te ions.

The potentiodynamic \(j/E\) profiles of a n-Si electrode in a 5 mM TeO₂ + 0.5 M H₂SO₄ solution in the dark are shown in Fig. 3. To facilitate discussion of the voltammetric data, the following notation is used: individual voltammetric waves are labelled with a combination of arabic numerals and a lower case letter, either “a” or “c”, denoting anodic and cathodic processes, respectively. The use of the same arabic numeral for a set of voltammetric waves denotes correlated processes. A wide cathodic peak 1c, at ca. −0.530 V vs. SCE is observed during the first negative scan which corresponds to reaction (1). Extending the scan towards more negative potentials, a small shoulder 2c is observed at ca. −0.680 V which is probably related to the reduction of Te to H₂Te [47], but no anodic process are defined during the positive potential excursion. An interesting feature is that after the second potential scan peak 1c is shifted towards more positive potentials (−0.350 V vs. SCE), indicating that a nucleation overpotential is required for the nucleation of tellurium islands on the silicon substrate. This means that it is easier to deposit Te when a layer of the element is covering the Si surface. Also noticeable is the increase in the cathodic peak 2c attributed to Te²⁻ formation and its corresponding re-oxidation which is evident from through the appearance

![Fig. 2. Energy band diagram for n-type silicon (1 0 0) in contact with an aqueous solution at \( \text{pH} = 0 \), containing the redox couple HTeO₂⁺/Te⁻ (only the empty HTeO₂⁺ levels are shown). Tellurium deposition can be achieved through electron transfer from the conduction band to the solution.](image1)

![Fig. 3. Potentiodynamic profiles of the polished side of a n-Si (1 0 0) electrode in 5 mM TeO₂ + 0.5 M H₂SO₄. Scan rate: 0.005 V s⁻¹. (-- --) first cycle; (---) second cycle. The arrows denote the direction of the potential scan. Roman numbers I and II behind peak 1c indicate position of this peak in the first and second scan, respectively. Refer to text for peak notation.](image2)
of an anodic peak 2a at ca. ~0.650 V during the positive potential excursion. The latter can be visualized as an anodic process superimposed on a cathodic one. As in the first scan, no stripping processes are observed, indicating that tellurium deposition onto n-type silicon is not reversible. This can be due to two effects [48]: first, the density of holes in the valence band is very low (in dark conditions), thus the oxidation rate due to valence band holes is very low; second, the barrier height of the n-Si(1 0 0)/Te contact is very large (ca. 0.8 eV [49]), thus the rate of thermal oxidation of electrons from the tellurium into the silicon conduction band is very low.

In the presence of Cd\(^{2+}\) (see Fig. 4), the voltammogram shows that cadmium deposition starts at a potential of ~0.725 V, and the large current density increase at peak 1c results from the large Cd\(^{2+}\) concentration of the solution (0.5 M). A wide anodic peak 1a corresponding to the metal stripping can be seen in the positive voltammetric scan. Further, the presence of a current loop, typical of a nucleation-growth process at the electrode surface, is also observed.

To demonstrate the influence of the rough face in the electrochemical behavior, voltammograms for each of the two faces of a n-Si(1 0 0) wafer electrode were recorded. Fig. 5 shows these voltammograms done in an electrodeposition bath containing both CdTe precursors in the presence of 0.5 M NH\(_4\)F, at a temperature of 85 °C. During the negative scan of the polished side, a small cathodic peak 1c appears at ~0.260 V which can be associated with the reduction of HTeO\(_2^+\) to tellurium.

![Fig. 4. Cyclic voltammogram of the polished side of a n-Si (1 0 0) electrode in 0.5 M CdSO\(_4\) + 0.5 M H\(_2\)SO\(_4\). Scan rate: 0.005 V s\(^{-1}\). The arrows denote the direction of the potential scan. Refer to text for peak notation.](image)

The compound electrodeposition is related to the broad current peak 2c at ~0.380 V, followed by a current decay which is extended until ~0.620 V. Beyond this value, the cathodic current increases almost linearly with potential (3c), a process associated with the deposition of metallic Cd that is present in a substantial concentration in the bath. The small peak 3a observed during the positive scan indicates that only a fraction of the electrodeposited Cd is stripped, probably because the remaining cadmium is hindered under a CdTe layer. Due to the presence of a Schottky barrier at the n-Si(1 0 0) surface, the anodic stripping of CdTe is not observed. During the positive scan the current remains cathodic indicating a lower electrodeposition overvoltage on an already coated surface.

The cyclic voltammetric response of the rough face of n-Si(1 0 0) in the same electrodeposition bath is also depicted in Fig. 5. In general, this system presents the same voltammetric features and the same electrochemical trends of its opposite polished side. However, according to its textured nature and the correspondingly greater electrode surface area, higher current densities are observed. A negative shift of peak I, which now appears as a shoulder forming a broad band with peak 2c, is also observed. Deposition of CdTe containing a Te excess can occur within this potential region. From ~0.500 V and before metallic cadmium deposition, i.e. ~0.600 V, stoichiometric CdTe deposition can be expected. In fact, EDS analysis shows that, in this interval, CdTe thin
films with Cd/Te atomic ratios close to 1 are obtained (vide infra). Moreover, due to a greater electrodic surface area, current peaks corresponding to cadmium deposition (3c) and cadmium stripping (3a) are enhanced on this rough surface.

3.3. CdTe electrodeposition at constant potential

Cd + Te thin films were prepared at 85 °C using constant potential electrodepositions on n-Si(1 0 0) substrates at potentials ranging from −0.500 to −0.700 V from a 5 mM TeO₂ + 0.5 M CdSO₄ + 0.5 M H₂SO₄ + 0.5 M NH₄F solution. For all the deposition experiments, about the same charge density was used to ensure that the nominal thickness of these deposits (≈1 μm) would be relatively constant. The compositions of the Cd + Te thin films were estimated by EDS analysis. From the latter, it is inferred that the cadmium content increases as the potential is made more negative, which agrees with the thermodynamic electrodeposition potentials (HTeO₂⁻/Te, \( E^0 = +0.278 \) V; Cd²⁺/Cd, \( E^0 = −0.644 \) V). Cd + Te films with near stoichiometric compositions are obtained around −0.575 V vs SCE.

Fig. 6 shows the X-ray diffraction pattern of an as-electrodeposited CdTe thin film/n-Si(1 0 0) heterostructure, potentiostatically grown at −0.575 V at 85 °C and, the corresponding JCPDS pattern for cubic CdTe. All the diffraction peaks of Fig. 6(a) can be assigned to that of CdTe or Si substrate. This is an indication that the film is mainly composed of polycrystalline CdTe. It can be seen that the as-deposited film is well crystalized with a preferential orientation along the cubic [1 1 1] direction, which is characteristic of the usual spontaneous texture axis of electrodeposited CdTe. Furthermore, the ratios of intensities from the JCPDS file for CdTe indicate [1 1 1]/[2 2 0] and [1 1 1]/[3 1 1] ratios of 1.7 and 3.3, respectively, while the corresponding ratios for the deposit are closer to 3.0 and 4.0, respectively, suggesting a strong preferential [1 1 1] growth. Fig. 7(a)
shows the as received AFM image surface structure of the rough face of a n-Si(1 0 0) where the presence of inverted pyramids can be observed. According to Table 2, there is no significant difference between the roughness coefficient in the two sides of the Si wafer but, due to the presence of the pyramids, the RMS values are remarkably different. Fig. 7(b) shows an AFM image of an as-grown electrodeposited CdTe film (1 μm thickness, $E_{\text{dep}} = 0.575$ V), onto this rough silicon surface. The film presents a smooth aspect, with a cauliflower microstructure. Through the section analysis in AFM images, Fig. 7(c), it is deduced that the vertical height between the valleys and the summit of the inverted truncated pyramids in the rough silicon surface is on average, 500 nm. Then, a CdTe deposit, 1 μm, thick not only covers the substrate irregularities, but finally leads to a homogenous deposit. As is confirmed by the XRD analysis, the latter does not necessarily follow the substrate crystalline structure.

### 3.4. X-ray photoelectron spectroscopy (XPS) study

XPS measurements have been carried out for the as-electrodeposited sample surface and after several sequences of 4 keV Ar$^+$ sputtering. Ar sputtering reduces the amount of adventitious hydrocarbons on the sample surface but also leads to changes in composition as, for instance, by preferential loss of oxygen species due to the 4 keV Ar$^+$ bombardment [50]. After a certain sputter time, a steady state situation in the composition in the so-called altered layer is reached. For our sample, this was the case after about 10 min of 4 keV Ar$^+$ sputtering. Fig. 8 shows the Te 3d and Cd 3d spectra for this situation. Also only one Cd 3d doublet is seen but two Te 3d doublets, indicating that Te is present in the electrodeposited film in at least two chemical states. Chemical state fitting to the Te 3d signal revealed three chemical bonds to be involved, corresponding to phases of CdTe, TeO$_2$ and elemental Te. These bonds are indicated with their Te 3d$5/2$ binding energies [46] in Fig. 8, taking the binding energy reference at 404.9 eV for Cd 3d$3/2$. The results of Te 3d spectra fitting for the as-introduced sample and after 1 and 10 min of 4 keV Ar$^+$ sputtering are summarized in Table 3. Table 4 shows the percentages of type of chemical bonding with Te for the three situations derived from the fittings. As can be seen in Table 3, Te is found in the surface of the as-introduced sample chemically bonded to Cd and O. Hence, at the sample

### Table 2

<table>
<thead>
<tr>
<th>Material</th>
<th>Geometric area (μm²)</th>
<th>Surface area (μm²)</th>
<th>Roughness coefficient</th>
<th>RMS (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat-Si</td>
<td>100.00</td>
<td>100.00</td>
<td>1.0000</td>
<td>1.698</td>
</tr>
<tr>
<td>Rough-Si</td>
<td>100.00</td>
<td>102.66</td>
<td>1.0266</td>
<td>191.000</td>
</tr>
<tr>
<td>Rough-Si/CdTe</td>
<td>100.00</td>
<td>112.36</td>
<td>1.1236</td>
<td>32.490</td>
</tr>
</tbody>
</table>

### Table 3

<table>
<thead>
<tr>
<th>Bond</th>
<th>Centre (eV)</th>
<th>FWHM (eV)</th>
<th>4 keV Ar$^+$ sputter time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Te–Cd</td>
<td>572.33</td>
<td>1.72</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>572.20</td>
<td>1.81</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>572.17</td>
<td>1.68</td>
<td>10</td>
</tr>
<tr>
<td>Te–Te</td>
<td>–</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>573.54</td>
<td>2.00</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>573.42</td>
<td>1.65</td>
<td>10</td>
</tr>
<tr>
<td>Te–O</td>
<td>575.66</td>
<td>1.95</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>575.35</td>
<td>2.18</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>575.68</td>
<td>2.01</td>
<td>10</td>
</tr>
</tbody>
</table>

### Table 4

<table>
<thead>
<tr>
<th>4 keV Ar$^+$ sputter time (min)</th>
<th>Te–Cd</th>
<th>Te–Te</th>
<th>Te–O</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>47</td>
<td>0</td>
<td>53</td>
</tr>
<tr>
<td>1</td>
<td>61</td>
<td>20</td>
<td>19</td>
</tr>
<tr>
<td>10</td>
<td>75</td>
<td>13</td>
<td>12</td>
</tr>
</tbody>
</table>
surface CdTe and TeO₂ are present, and, according to Table 4, in approximately equal amounts. After sputtering, Te–Te bonds appear due to 4 keV Ar⁺ bombardment induced reduction of TeO₂. As a consequence, the amount of CdTe detected by XPS increases with increasing sputter time (see Table 4). Likewise, the amount of Te–O bonds decreases. As elemental Te comes from the ion bombardment induced chemical reduction of TeO₂, the amount of Te–Te bonds is high for the first sequences of Ar sputtering and drops with the decrease of Te–O bonds present in the ion bombardment altered layer. In the steady state situation, about 75% of Te is found as CdTe. On the other hand, the Cd 3d signal does not give much scope for data interpretation since the Cd 3d5/2 peak is at 404.9 eV in CdTe, 405.0 eV in elemental Cd and 405.2 eV in CdO [46], showing thus, very small chemical shifts. It is worthwhile to mention that it has been reported that the exposure of CdTe to air leads to surface oxidation with the formation of TeO₂ and CdO and that these surface oxides can be removed by Ar sputtering. [51,52]. Furthermore, only very weak preferential sputtering of Cd atoms, which has been shown to be largely independent of ion mass and ion energy, is documented for CdTe [53]. No diffusion or segregation effects were reported, and good LEED patterns were obtained even after ion bombardment indicative of a crystalline CdTe surface and good LEED patterns were obtained even after ion bombardment indicative of a crystalline CdTe surface layer [54]. However, in our sample we found Te–O bonds even after prolonged Ar sputtering. Hence, we conclude from the XPS study that, at the sample surface, CdTe and TeO₂ are present in similar amounts; inside the electrodeposited film, the majority phase is CdTe but also Te–O bonds are present. A possible explanation could be that the oxygen contamination inside the electrodeposited CdTe film is due to reaction with water in the electrolyte solution and thus has been incorporated into the film as TeO₂ [55].

4. Conclusions

We have shown that the rear side of an n-type (1 0 0) Si wafer polished on one side can be successfully employed as a substrate for the electrodeposition of uniform and compact morphology CdTe films from a plating bath containing 5 mM TeO₂, 0.5 M CdSO₄, 0.5 M H₂SO₄ and 0.5 M NH₄F. The EDS and XRD analyses demonstrate that the as deposited films obtained at −0.575 V presented a near stoichiometric composition and also were well crystallized with a preferential orientation along the [1 1 1] cubic direction. The XPS study revealed that, at the sample surface, CdTe and TeO₂ are present in similar amounts and that inside the electrodeposited film the majority phase is CdTe but also Te–O bonds are present. Probably the oxygen contamination inside the electrodeposited CdTe film is due to reaction with water in the electrolyte solution and thus has been incorporated into the film as TeO₂.

Acknowledgements

This work has been supported by FONDECYT(Chile) project No. 8000022. E.A.D. thanks CSIC (Universidad de la República) and PEDECIBA-Ética, UNESCO (Uruguay). D.L and J.R.R.-B thank CYCIT (España) and UE (MAT2000-1505).

References
